REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have canceled claims 15-18 and 28-39 without prejudice or disclaimer. In addition, Applicants have amended the remaining claims to recite a Pb-free solder (rather than a Pb-free solder comprising Bi), and to recite that the Sn-Bi alloy layer includes 1-5 wt% Bi (rather than 1-20 wt% Bi). Moreover, claim 1 has been further amended to recite that the Sn-Bi alloy layer is formed as a surface layer on the lead; and claims 6 and 19 have been further amended to recite that the Sn-Bi alloy plating layer is directly formed as a surface layer.

Furthermore, new claims 40-59 are being added to the application. Of these newly added claims, claims 43, 50, 51 and 59 are independent claims, each directed to an electronic device, and will be discussed infra.

Claims 40 and 41, each dependent on claim 1, respectively recites that the lead is made of a Cu alloy and recites that the lead is made of an Fe-Ni alloy; and claim 42, also dependent on claim 1, recites that the lead is made of an Fe-Ni alloy, with a copper layer provided between the lead and the Sn-Bi alloy layer.

New independent claim 43 recites an electronic device having a first electrode provided on an electronic component and a second electrode formed on a circuit board, the two electrodes being electrically connected with each

other by means of a solder, with an Sn-Bi alloy layer containing 1-5 wt% Bi being on the first electrode, and this alloy layer being in contact with the solder which is made of a Pb-free alloy, the solder being in contact with the second electrode. Claims 44 and 45, each dependent on claim 43, respectively recites that there is a Cu layer between the first electrode and the alloy layer, and recites that the first electrode is made of a Cu alloy; and claim 46, also dependent on claim 43, recites that the first electrode is made of an Fe-Ni alloy. Claims 47 and 48, each dependent on claim 43, respectively define elemental components of the solder; and claim 49, also dependent on claim 43, recites that the first and second electrodes are bonded with each other by a bonding part including components of specific elements.

Independent claim 50 defines an electronic device having a first electrode provided on an electronic component and a second electrode provided on a circuit board on which the electronic component is mounted, the two electrodes being bonded with each other by means of a solder, and wherein an Sn-Bi alloy layer containing 1-5 wt% Bi is adjacent the first electrode as a surface layer and this alloy layer is in contact with the solder, made of lead-free alloy, the solder being in contact with the second electrode.

Independent claim 51 defines an electronic device which includes an electronic component having a first electrode with an Sn-Bi alloy layer, a circuit board with a second electrode, and a bonding part of a lead-free solder which

bonds the first and second electrodes to each other, the alloy layer containing 1-5 wt% Bi and being on the first electrode, with the lead-free solder being in contact with the second electrode. Claims 52 and 53, each dependent on claim 51, respectively recites that a Cu layer is provided between the first electrode and the Sn-Bi alloy layer, and recites that the first electrode is made of a Cu alloy; and claim 54, also dependent on claim 51, recites that the first electrode is made of an Fe-Ni alloy. Claims 55 and 56, each dependent on claim 51, each defines components of the Pb-free solder; and claims 57 and 58, each dependent on claim 51, respectively defines elemental components of the bonding part, and recites that the electronic component is a semiconductor.

Claim 59 defines an electronic device which includes a semiconductor provided with a first electrode, and a second electrode formed on a circuit board, the two electrodes being electrically connected with each other by means of a solder, and wherein an Sn-Bi alloy layer containing 1-5 wt% Bi is adjacent the first electrode as a surface layer, and this alloy layer is in contact with the solder, made of a Pb-free alloy, with the solder being in contact with the second electrode.

In connection with the amendments to previously considered claims, and in connection with the newly added claims, note, for example, pages 4-6 of Applicants' specification, together with the examples in Applicants' specification beginning at page 18 of Applicants' specification. Note also, for

example, Fig. 4, showing, for example, Sn-1 Bi and Sn-5 Bi for the metallized layer. Note also corresponding disclosures of Sn-1 Bi and Sn-5 Bi in Figs. 5-8 of Applicants' disclosure.

The objection to claim 35 in Item 3 on page 2 of the Office Action mailed December 17, 2001, is noted. This objection is moot in light of canceling of claim 35.

The provisional rejection of claims 1-39 under the judicially created doctrine of obviousness-type double patenting, over claims 1-13 of application Serial No. 09/581,631, filed June 15, 2000m, is respectfully traversed, especially insofar as applicable to the claims as presently amended in the above-identified application, and as amended in No. 09/581,631.

That is, it is respectfully submitted that the present claims recite, for example, the Sn-Bi alloy layer as a surface layer on specified leads. It is respectfully submitted that in the present claims, there are set forth relationships among the leads (electrodes), the Sn-Bi alloy layer and the solder, which would have neither been disclosed nor suggested by the subject matter claimed in No. 09/581,631. Accordingly, it is respectfully submitted that the obviousness-type double patenting rejection (provisional) is improper, and reconsideration and withdrawal of the provisional double patenting rejection is respectfully requested.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the documents used by the Examiner in rejecting claims in the Office Action mailed December 17, 2001, that is, the teachings of U.S. Patent No. 6,110,608 to Tanimoto, et al., International (PCT) Published Application No. WO99/30866 (Shimokawa, et al.), Japanese Published Application No. 8-132277, and Japanese Published Application No. 10-41621, under the provisions of 35 USC 102 and 35 USC 103.

Initially, the International published application of Shimokawa, et al. is noted. It is respectfully submitted that, as the claims are presently amended, Applicants clearly have support, within the meaning of 35 USC 112, first paragraph, for the presently claimed subject matter, including the subject matter of claims 1, 3-6, 8-11, 14, 19, 21-24 and 27. That is, the claims have been amended to recite a Pb-free solder, rather than a Pb-free solder comprising Bi. It is respectfully submitted that claims including the recited solder have support in the International application of Shimokawa, et al., as well as in the Japanese priority application for the above-identified application, and that Shimokawa, et al. is not prior art.

In addition, claims reciting the negative limitation "without any plating layer between the lead and the Sn-Bi alloy plating layer", or reciting "without

any other plating under-layer" (see claim 15), have been deleted from the present application.

In view of the foregoing, it is respectfully submitted that all remaining claims have continuing support through prior applications of the above-identified application, and through the International (PCT) application of Shimokawa, et al., such that Shimokawa, et al. does not constitute prior art in connection with the presently claimed subject matter. Accordingly, reconsideration and withdrawal of Shimokawa, et al. as prior art in connection with the presently claimed subject matter, is respectfully requested.

As for the remaining applied references, attention is respectfully directed to Japanese Patent Document No. 10-41621, having a publication date of February 13, 1998. However, note that the above-identified application claims priority under 37 CFR 1.55 and 35 USC 119, of Japanese Priority Application No. 9-346,811, filed in Japan on December 16, 1997 (prior to the publication date of No. 10-41621). Applicants have claimed priority based upon No. 09-346811, in the Claim for Priority filed October 9, 2001 in the above-identified application. Moreover, this Claim for Priority filed October 9, 2001 indicates that the certified copy of the priority document was received in No. 09/581,631 in the national stage application No. 09/581,631, from the International Bureau.

Furthermore, Applicants submitted an English translation of the Japanese priority application, together with a Statement as to the accuracy of the

translation, with the Amendment submitted January 9, 2002 in No. 09/581,631. A copy of this English translation of the Japanese priority application, together with Statement of Accuracy thereof, is enclosed herewith.

It is respectfully submitted that the enclosed English translation establishes that the Japanese priority application for the above-identified application supports the presently claimed subject matter within the meaning of the first paragraph of 35 USC 112.

In view of all of the foregoing, it is respectfully submitted that Applicants have established that the above-identified application should be accorded benefit of the filing date of the Japanese priority application for the above-identified application, in connection with the presently claimed subject matter; that such filing date of the Japanese priority application is prior to the date, for prior art purposes, of No. 10-41621; and that, accordingly, No. 10-41621 does not constitute prior art in connection with the presently claimed subject matter. Accordingly, reconsideration and withdrawal of all rejections utilizing the teachings of No. 10-41621, is respectfully requested.

In view of all of the foregoing, it is respectfully submitted that the rejections under 35 USC 102/103 as set forth in Items 7, 13 and 20 are clearly improper. Accordingly, reconsideration and withdrawal of these rejections are respectfully requested. No further discussion of these rejections is necessary.

The remaining prior art rejections, set forth in Items 9, 11, 16 and 18, of the Office Action mailed December 17, 2001, are noted. However, in view of the canceling of claims by the present Amendment, it is respectfully submitted that the rejections as set forth in Items 9, 11 and 18 are clearly moot. Accordingly, no further discussion of these rejections is necessary.

In view of all of the foregoing, it is respectfully submitted that the sole remaining prior art rejection is that of pending claims over the teachings of Tanimoto, et al., as set forth in Item 16 on page 7 of the Office Action mailed December 17, 2001.

In connection with this rejection, it is respectfully submitted that the teachings of this reference would have neither disclosed nor would have suggested such an electronic device as in the present claims, utilizing a Pb-free solder, and having a lead of an electronic component (e.g., semiconductor device) on which an Sn-Bi alloy layer comprising 1-5 wt% Bi is formed as a surface layer. See, e.g., claims 1, 6, 11, 19, 24, 50 and 59.

Moreover, it is respectfully submitted that this reference as applied by the Examiner would have neither taught nor would have suggested such an electronic device as in the present claims, having the specified alloy layer as a surface layer, and wherein this alloy layer is directly formed as a surface layer. Note, e.g., claims 6, 11, 19 and 24.

Furthermore, it is respectfully submitted that this applied reference (Tanimoto, et al.) would have neither taught nor would have suggested such an electronic device as in the present claims, with the Sn-Bi alloy layer on the first electrode and in contact with the solder made of a Pb-free alloy, and the solder is in contact with the second electrode. See claim 43; note also claims 50 and 59.

Moreover, it is respectfully submitted that this reference would have neither taught nor would have suggested such an electronic device as in the present claims, utilizing the above-mentioned alloy layer, and wherein the alloy layer is on the first electrode and the Pb-free solder is in contact with the second electrode. See claim 51.

In addition, it is respectfully submitted that the teachings of Tanimoto, et al. would have neither disclosed nor would have suggested the other aspects of the present invention as in the remaining claims, including specific materials of the electrode as in, for example, claims 11, 19, 24, 45, 46, 53 and 54; and/or wherein a copper layer is provided between the first electrode and the Sn-Bi alloy layer, as in, for example, claims 44 and 53.

The invention as claimed in the above-identified application is directed to an electronic device utilizing a lead-free solder, the electronic device having components (e.g., a semiconductor device, circuit board, substrate, etc.) with respective electrodes, wherein the electrodes have good bonding properties

therebetween and good electrical contact, while avoiding formation of whiskers. Applicants have found that by utilizing a Sn-Bi plating layer on the first electrode structure as a surface layer, and/or, e.g., on the first electrode and in contact with the solder, the solder being in contact with the second electrode, this alloy layer including 1-5 wt% Bi, good wettability of the solder and a high strength bond are achieved, while avoiding whisker formation. As to effects achieved according to the present invention, note, for example, Figs. 4-7 of Applicants' disclosure, showing advantages achieved by the present invention in strength and wettability.

Tanimoto, et al. discloses a lead material for an electronic part, and a lead and semiconductor device using such material. The described structure has a lead material with a first plated layer and a second plated layer provided on a surface of a conductive substrate in this order, a melting temperature of the material of the second plated layer being lower than that of a material of the first plated layer. See column 2, lines 43-49. This patent discloses that the lead material for the electronic part can include a first plated layer made of a Sn substance and a second plated layer made of a Sn alloy containing at least one element selected from a group of Ag, Bi, Cu, In and Zn; or, alternatively, the first plated layer can be made of a Sn alloy containing at least one element selected from a group of Ag, Cu, Sb and Y and a second plated layer made of a Sn substance. See column 2, lines 50-60. As to the Sn-Bi alloy, this patent

discloses that the Bi percentage content can be up to 87wt%. See column 4, lines 23-27. However, this patent further discloses that if the lead material provides junction with a solder and 20wt% or more Bi exists at the solder part, the junction strength of the solder part gradually deteriorates, so that the alloy composition is preferably adjusted such that the Bi percentage content at the junction part after soldering is 20wt% or less. This patent further discloses that an Sn-Bi alloy having a Bi content of 30wt% or less as the Sn alloy is generally preferred. See column 4, lines 48-62.

Initially, the alternative embodiments of the invention described in Tanimoto, et al., are noted. Where the tin alloy contains bismuth, it constitutes the second plated layer (spaced from the lead material); in contrast, where the tin alloy is adjacent the lead material (is the first plated layer), the alloying element is selected from a group of Ag, Cu, Sb and Y (that is, not including Bi). Taking the teachings of Tanimoto, et al. as a whole, as required under 35 USC 102 and 35 USC 103, it is respectfully submitted that Tanimoto, et al. would have neither taught nor would have suggested, and in fact would have taught away from, the presently claimed subject matter, wherein the Sn-Bi alloy layer is provided on the first electrode structure as a surface layer; or is in contact with the solder and on the, e.g., first electrode structure (e.g., either the electrode of Cu (Cu alloy) or Fe-Ni alloy or a Cu layer on the electrode). That is, it is respectfully submitted that Tanimoto, et al. teaches that the tin alloy is

on the tin substance when the alloy contains bismuth, which is different from the present invention.

In addition, note that Tanimoto, et al. discloses amounts of bismuth in the Sn-Bi alloy up to 87wt%, and includes preferred amounts of 30wt% or less. It is respectfully submitted that the teachings of Tanimoto, et al., including amounts of bismuth in the Sn-Bi alloy preferably of up to 30wt%, would have taught away from the present invention including the Sn-Bi alloy layer containing 1-5wt% Bi, and advantages achieved thereby as shown in, for example, Figs. 4-7 of the present disclosure.

Reference by the Examiner to specific examples of Tanimoto, et al., in Item 17 on page 7 of the Office Action mailed December 17, 2001, is noted. The examples must be taken in light of the teachings of Tanimoto, et al. as a whole, including the broad description of the invention therein as described in column 2, and referred to previously, with respect to the tin alloy. Taking the teachings of Tanimoto, et al. as a whole, as discussed previously, including comparing the alternative embodiments, it is respectfully submitted that this reference would have taught away from the present invention including the Sn-Bi alloy layer on the first electrode structure, in particular adjacent the first electrode structure, and/or with amount of bismuth in the Sn-Bi alloy layer as in the present claims, especially with the Sn-Bi alloy in contact with the solder (PB-free solder).

In view of the foregoing comments and amendments, reconsideration and allowance of all claims remaining in the application are respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. This marked-up version is on the attached pages, the first page of which is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 500.38665CX1) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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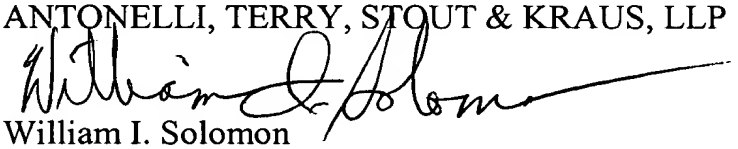

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel claims 15-18 and 28-39 without prejudice or disclaimer, and amend the claims remaining in the application as follows:

1. (Amended) An electronic device comprising a substrate and a semiconductor device, which are connected with each other by means of a Pb-free solder [comprising Bi], the semiconductor device having a lead on which an Sn-Bi alloy layer comprising 1 to [20] 5 wt% Bi is formed as a surface layer.

2. (Amended) An electronic device according to claim 1, wherein the Pb-free solder [comprising Bi] is an Sn-Ag-Bi alloy.

6. (Amended) An electronic device comprising a substrate and a semiconductor device, which are connected with each other by means of a Pb-free solder [comprising Bi], the semiconductor device having a lead [made of Cu or a Cu alloy] on which an Sn-Bi alloy plating layer comprising 1 to [20] 5 wt% Bi is directly formed as a surface layer.

7. (Amended) An electronic device according to claim 6, wherein the Pb-free solder [comprising Bi] is an Sn-Ag-Bi alloy.

11. (Amended) An electronic device comprising a substrate and a semiconductor device, which are connected with each other by means of a Pb-free solder [comprising Bi], the semiconductor device having a lead made of Cu or a Cu alloy on which an Sn-Bi alloy layer comprising about 1 to about [20] 5 wt% Bi is directly formed as a surface layer.

12. (Amended) An electronic device according to claim 11, wherein the Pb-free solder [comprising Bi] is an Sn-Ag-Bi alloy.

19. (Amended) An electronic device comprising a substrate and a semiconductor device, which are connected with each other by means of a Pb-free solder [comprising Bi], the semiconductor device having a lead made of an Fe-Ni alloy on which an Sn-Bi alloy plating layer comprising 1 to [20] 5 wt% Bi is directly formed as a surface layer.

20. (Amended) An electronic device according to claim 19, wherein the Pb-free solder [comprising Bi] is an Sn-Ag-Bi alloy.

24. (Amended) An electronic device comprising a substrate and a semiconductor device, which are connected with each other by means of a Pb-free solder [comprising Bi], the semiconductor device having a lead made of an

Fe-Ni alloy on which an Sn-Bi alloy layer comprising about 1 to about [20] 5 wt% Bi is directly formed as a surface layer.

25. (Amended) An electronic device according to claim 24, wherein the Pb-free solder [comprising Bi] is an Sn-Ag-Bi alloy.